Notice of Allowability	Application No.	Applicant(s)	
	10/621,364	YANAGI ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 21 November 2006*.

2. ☒ The allowed claim(s) is/are *1-22*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew Waxman on 21 December 2006.

2. The application has been amended as follows:

Please amend claim 1 as follows:

1. A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal based on at least a base clock signal, the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b)

stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period; and

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal and the base clock signal; wherein

the driving control circuit stops driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintains driving for obtaining at least one of the control clock signal and the base clock signal ~~the clock signals other than the clock signal~~, and

the base clock signal, the clock signal and the control clock signal have different speeds.

Please amend claim 2 as follows:

2. A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for

scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits and maintaining driving for obtaining at least one of the control clock signal and a base clock signal ~~clock signals other than the clock signal~~;

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and the driving control circuit stops driving of the output timing clock generation circuit in the inaction period, and

the output timing clock, the control clock signal and the clock signal have different speeds.

Please amend claim 3 as follows:

3. A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintaining driving for obtaining at least one of the control clock signal and a base clock signal ~~clock signals other than the clock signal~~;

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits; and

a start timing clock generation circuit for generating a start timing clock which is used as a scanning start timing signal of the driving circuits,

wherein:

the output timing clock generation circuit generates the output timing clock based on the start timing clock generated in the start timing clock generation circuit, the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit and the driving control circuit stops driving of the start timing clock generation circuit in the inaction period, based on the control clock signal, and

the start timing clock, the control clock signal and the clock signal have different speeds.

Please amend claim 4 as follows:

4. A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal based on a base clock signal, the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period

being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal, the clock signal being used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintaining driving for obtaining at least one of the control clock signal and the base clock signal ~~clock signals other than the clock signal~~; wherein

the clock signal generation circuit is a clock signal oscillation circuit for oscillating a clock signal, and

the control clock signal, the clock signal and the base clock signal have different speeds.

Please amend claim 6 as follows:

6. A driving method for a display device which selects each line of a screen having pixels aligned in a matrix manner by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, the driving method comprising:

generating, as a driving control signal, a control clock signal based on at least a base clock signal, the control clock signal defining an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen;

stopping driving of a clock signal generation circuit in the inaction period, while maintaining driving for obtaining at least one of the control clock signal and the base clock signal ~~clock signals other than the clock signal~~, the clock signal generation circuit being for

generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal and the base clock signal; wherein

the base clock signal, the control clock signal and the clock signal have different speeds.

Please amend claim 7 as follows:

7. A display device which selects each line of a screen having pixels aligned in a matrix manner and provided in a display section by applying a scanning signal to a scanning signal line of a pixel of each line so as to scan the screen, and supplies a data signal from a data signal line to a pixel of a selected line so as to carry out display, comprising:

a driving control circuit which (a) generates, as a driving control signal, a control clock signal that defines an inaction period where all scanning signal lines become non-scanning state, the inaction period being provided between scanning periods for scanning the screen, and which (b) stops driving of driving circuits provided for driving the display section, the driving control circuit stopping driving of the driving circuits in the inaction period;

a clock signal generation circuit for generating a clock signal which is used for taking the data signal into the data signal line, the clock signal being faster than the control clock signal;

the driving control circuit stopping driving of the clock signal generation circuit in the inaction period, in addition to stopping driving of the driving circuits, and maintaining driving for obtaining at least one of the control clock signal and a base clock signal ~~clock signals other than the clock signal~~; and

an output timing clock generation circuit for generating an output timing clock which is used as an output timing signal of a driving signal to the display section from the driving circuits,

wherein:

the clock signal generation circuit generates the clock signal based on the output timing clock generated by the output timing clock generation circuit, and

the control clock signal, the clock signal and the output timing clock have different speeds.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

21 December 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER